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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/777,694	02/07/2001	Kazutami Arimoto	49657-994	4365

7590 08/11/2003

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EXAMINER
YOHA, CONNIE C

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 08/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/777,694	Applicant(s) ARIMOTO ET AL.	
	Examin r Connie c. Yoha	Art Unit 2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) *13-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 February 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

1. Examiner took notice of the remarks and amendments made by applicant filed on 6/4/03.

2. A second non-final rejection is applied to the pending claims using newly cited reference.

\ Response to Amendment

3. This office action is in response to Amendment filed on 6/4/03.

Claim 1, 6, and 9 are amended.

Claims 1-12 are pending.

Withdrawn of allowability

4. The indicated allowability of claim 5-7 are withdrawn in view of the newly discovered reference(s). Rejection based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Inagaki, Pat, No. 4716551.

With regard to claim 1, Inagaki discloses a memory array (fig. 1, 23) including a plurality of memory cells arranged in a matrix; a refresh timer circuit (fig. 1, 52) providing a refresh request signal (fig. 1, /RFSH) at a time interval required to refresh data held by the plurality of memory cells; a command generation circuit (fig. 1, 50) generating an internal command signal in response to an access command (col. 3, line 25-41) (col. 4, line 19-28); and a row selection control circuit (fig. 1, 10) carrying out an operation associated with row selection of the memory array, the row selection control circuit including: a timing control circuit (fig. 1, 25) rendered active in response to the internal command signal (/RAS, /CAS, /WE) to output a timing signal (fig. 1, AL) of a row selection operation of the memory cell (col. 3, line 24-41), a refresh control circuit (fig. 1, 28) receiving and holding the refresh request signal (fig. 1, /RFSH) to output an internal refresh command (fig. 1, RF) when the timing control circuit attain an inactive state (when /CAS and /WE is not enable) (col. 4, line 29-37), a refresh timing control circuit (fig. 1, 25,30, 32) (in response to the internal refresh command signal (fig. 1, RF) to output the timing signal instead of the timing control circuit (col. 4, line 32-56); and a row selection circuit (fig. 1, 21) carrying out row selection of the memory cell in response to the timing signal.

With regard to claim 2, Inagaki discloses wherein the access command includes a read out command (fig. 1, OE), wherein a basic cycle time staring from reception of the access command by the memory device up to reception of the next access command is at least a total time of a normal read out cycle time starting from output of the internal command signal up to completion of data read out from the memory array

and a refresh cycle time starting from output of the internal refresh command signal up to completion of refresh of a portion in the memory array corresponding to the internal refresh command signal (fig. 3).

With regard to claim 3, Inagaki discloses wherein the refresh control circuit comprises a latch circuit (fig. 1, 28) receiving and hold the refresh request signal (fig. 1, RF), and a pulse generation circuit (fig. 1, 25) generating a pulse that becomes a basis of the internal command signal when an output of the latch circuit indicates input of the refresh request signal and the timing control circuit is rendered inactive (col. 4, line 29-54) (also with regard to claim 4-7).

With regard to claim 8, Inagaki discloses a data input/output control circuit (fig. 1, 26, 27) receiving and holding as read out data the output from the memory array, and receiving an output enable signal (fig. 1, OE) to output the read out data.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inagaki, Pat, No. 4716551 in view of Taguchi et al, Pat. No. 6438055 (previously cited).

With regard to claim 9, Inagaki as applied in prior rejection, disclosed all claimed subject matter including a refresh counter circuit (fig. 1, 29) sequentially updating and providing a refresh row address corresponding to a row to be refreshed, and a select circuit (fig. 1, 20) receiving the normal row address (fig. 1, A0-A7) and the refresh row address (from fig. 1, 29) as an address corresponding to row selection of the memory array in response to the internal refresh command signal (fig. 1, RF). However, Inagaki does not disclose wherein the row selection control circuit further comprises an address latch circuit holding an applied row address to output a normal row address. Taguchi however, discloses wherein the row selection control circuit comprises an address latch circuit (fig. 3, 14) holding an applied row address to output a normal row address. Therefore, it would have been obvious for one having an ordinary skill in the art at the time the invention was made to incorporate the use of an address latch circuit as taught by Taguchi's into Inagaki's for the purpose of holding or latching the incoming addresses location to be used by the selecting circuit.

With regard to claim 10, Inagaki, as applied in prior rejection, disclosed all claimed subject matter except the memory array includes of banks that allows a row select operation independently, wherein the refresh control circuit outputs the internal refresh command signal after the refresh control circuit is rendered inactive when a bank indicated by the normal row address coincides with a bank indicated by the refresh row address. However, Taguchi discloses the memory array includes of banks (fig. 3, Bank0, Bank1) that allows a row select operation independently, wherein the refresh control circuit outputs the internal refresh command signal after the refresh control

circuit is rendered inactive when a bank indicated by the normal row address coincides with a bank indicated by the refresh row address (col. 1, line 24-64). Therefore, it would have been obvious for one having an ordinary skill in the art at the time the invention was made to incorporate the plurality of banks structure as taught by Taguchi's into the Inagaki's to achieve the operation of normal and refresh operation of the memory array having plurality banks structures.

With regard to claim 11, Inagaki discloses the address latch circuit receives the applied row address in synchronization with a clock signal (col. 3, line 24-30) (also with regard to claim 12).

Conclusion

7. When responding to the office action, Applicants' are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

8. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02 (b)).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (703) 306-5731. The examiner can normally be reached on Mon. - Fri. from 8:00 A.M. to 5:30 PM. The examiner's supervisor, David Nelms, can be reached on (703) 308-4910. The fax phone number for this Group is (703) 308-7722. Any inquiry of a general nature or

relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-0956.

C. Yoha

August 2003

Connie C. Yoha

Patent Examiner

Art Unit 2818